



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Aveek Sarkar et al.

Title:

METHOD AND SOFTWARE FOR IMPROVED CIRCUIT PATH TIMING

PREDICTIONS, AND CIRCUIT DESIGN PRODUCED THEREWITH

Application No.: 10/651,113

Filed:

August 28, 2003

Examiner:

(Unassigned)

Group Art Unit:

2858

Atty. Docket No.: 004-8907

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PTO/SB/08B (Substitut	e for form 1449/PTO)	Attorney Docket No.:	004-8907				
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SEP 2 2 2005			Examiner Name:	(Unassigned)				
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NON PATENT LITERATURE DOCUMENTS								
Examiner Initials*	Cite No. ¹	Include name of author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.						
		"Synopsys and Texas Instruments", product description, 6 pages, Synopsys, Inc., copyright 1999.						
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		Agah, Hamid, "Physical Synthesis", Application Note: FPGAs, from XILINX®, XAPP140, (v1.0), 3 pages, Xilinx, Inc., February 26, 2001.						
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		Bray, Jeffrey, Sr., "Verifying timing of external IP key to SoC success", EE Times, May 28, 2002, 3 pages, downloaded from http://www.eetimes.com , May 14, 2003.						
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